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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,381	06/29/2004	Masatake Nakano	120164	9028
25944	7590	08/23/2006	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			ISAAC, STANETTA D	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/500,381

Applicant(s)

NAKANO, MASATAKE

Examiner

Stanetta D. Isaac

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 7-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the RCE and amendment filed on 7/27/06 and 6/13/06, respectively. Currently, claims 7-22 are pending.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/27/06 has been entered.

Claim Objections

Claim 8 is objected to because of the following informalities: On line 6, "+wafer" should read as "wafer". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7-10 and 19-22 are rejected under 35 U.S.C. 102(a/e) as being anticipated by Yokokawa et al., US Patent 6,959,854.

Yokokawa discloses the semiconductor method as claimed. See figures 1-9, and corresponding text, where Yokokawa teaches, pertaining to claim 7, a method of producing an SOI wafer comprising at least the steps of forming an insulator film **10** on at least one of a bond wafer **1** made of silicon single crystal to form an SOI layer and a base wafer **2** made of silicon single crystal to be a support substrate (figure 1A; col. 6, lines 53-60), bonding each main surface of the bond wafer and the base wafer via that insulator film (figure 1D; col. 7, lines 14-22), and making the bond wafer bonded to the base wafer thinner (figures 1E-G; col. 7, lines 24-40), wherein the base wafer is one silicon wafer selected from a group consisting of an epitaxial wafer, a nitrogen doped wafer, a hydrogen annealed wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer (col. 6, lines 53-57, epitaxial wafer).

Yokokawa teaches, pertaining to claim 8, a method of producing an SOI wafer comprising at least the steps of forming an insulator film **10** on at least one of a bond wafer **1** made of silicon single crystal to form an SOI layer and a base wafer **2** made of silicon crystal to be a support substrate (figure 1A; col. 6, lines 53-60), forming a micro bubble layer **11** in the bond wafer by implanting gas ions from a main surface of the bond wafer (figure 1A; col. 6, lines 58-65), bonding the ion-implanted main surface of the bond wafer to a main surface of the base wafer via the insulator film (figure 1D; col. 7, lines 14-22), and delaminating the bonded wafer at the micro bubble layer as a border (figures 1E-G; col. 7, lines 24-40), wherein the base wafer is one silicon wafer selected from a group consisting of an epitaxial wafer, a nitrogen

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doped wafer, a hydrogen annealed wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer (col. 6, lines 53-57, epitaxial wafer).

Yokokawa teaches, pertaining to claims 9 and 10, wherein one silicon wafer selected from a group consisting of an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped, and annealed wafer, and an entire N-region wafer is used as the bond wafer (col. 6, lines 53-57, epitaxial wafer).

Yokokawa teaches, pertaining to claims 19-22, an SOI wafer produced by the method of claims 7-10 (figure 1G; col. 7, lines 35-42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokokawa et al., US Patent 6,959,854.

Yokokawa discloses the semiconductor method substantially as claimed. See preceding rejection of claims 7-10 and 19-22 under 35 U.S.C. 102(a/e).

However, Yokokawa fails to show, pertaining to claims 11 and 12, wherein the SOI layer to be formed has a thickness of 0.3 μm or less. In addition, Yokokawa fails to show, pertaining to claims 13-18, wherein the insulator film to be formed has a thickness of 0.4 μm or less.

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Yokokawa teaches the formation of an SOI layer and an insulator film to produce a SOI wafer.

It would have been obvious to one of ordinary skill in the art to incorporate, wherein the SOI layer to be formed has a thickness of 0.3 μm or less; wherein the insulator film to be formed has a thickness of 0.4 μm or less, in the method of Yokokawa, pertaining to claims 11-18, according to the teachings of Yokokawa, with the motivation that, since Yokokawa teaches the formation of an SOI layer and an insulating film to produce a SOI wafer, one of ordinary skill in the art would be capable of forming the above thicknesses during routine experimentation, especially since no criticality has been shown.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
August 20, 2006



MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER